patent application number 09/640,870 entitled "Video and Graphics System with Video Scaling," U.S. patent application number 09/640,869 entitled "Video and Graphics System with a Data Transport Processor," U.S. patent application number 09/641,930 entitled "Video and Graphics System with a Video Transport Processor," U.S. patent application number 09/641,935 entitled "Video and Graphics System with Parallel Processing of Graphics Windows," and U.S. patent application number 09/642,510 entitled "Video and Graphics System with a Single-Port RAM," all filed August 18, 2000.

In the Claims:

Please cancel claims 4, 40 and 43-44 without prejudice, and add new claims 45-48. None of the claims has been amended in this response. All claims that are pending in the present application, namely, claims 1-3, 5-39, 41-42 and 45-48 are recited below for the Examiner's reference convenience.

1. A system on an integrated circuit chip comprising:

an MPEG video decoder for processing MPEG video data to generate video for displaying;

means for displaying the video; and

a system bridge controller having a north bridge function for coupling a CPU to a plurality of peripheral devices,

wherein the CPU and the plurality of peripheral devices are situated externally to the integrated circuit chip.

2. The system of claim 1 wherein the system bridge controller is capable of performing format conversion between big-endian data and little-endian data, between the CPU and one or more of the plurality of peripheral devices.

3. The system of claim 2 further comprising other components for processing video and graphics on the integrated circuit chip, and

wherein the system bridge controller is capable of performing format conversion between big-endian data and little-endian data, between the CPU and at least one of the MPEG video decoder, the means for displaying the video and the other components for processing video and graphics.

5. The system of claim 1 wherein the plurality of peripheral devices include one or more PCI devices, and wherein the system bridge controller includes a PCI bridge for coupling the CPU to the one or more PCI devices.

6. The system of claim 5 wherein the PCI bridge is capable of performing a DMA function between the one or more PCI devices and an external memory.

7. The system of claim 5 wherein the PCI bridge is capable of performing format conversion between big-endian data used in the CPU and little-endian data used in the one or more PCI devices.

8. The system of claim 5 wherein the PCI bridge is capable of performing format conversion between little-endian data used in the CPU and big-endian data used in the one or more PCI devices.

9. The system of claim 1 wherein the plurality of peripheral devices include one or more I/O devices, and wherein the system bridge controller includes an I/O bus bridge for coupling the CPU to the one or more I/O devices.

10. The system of claim 9 wherein the I/O bus bridge is capable of performing a DMA function between the CPU and the one or more I/O devices.

11. The system of claim 9 wherein the one or more I/O devices include a device selected from a group consisting of ROM, RAM, flash memory and 68000-compatible peripheral devices.

12. The system of claim 9 wherein the I/O bus bridge is capable of performing format conversion between big-endian data used in the CPU and little-endian data used in the one or more I/O devices.

13. The system of claim 9 wherein the I/O bus bridge is capable of performing format conversion between little-endian data used in the CPU and big-endian data used in the one or more I/O devices.

14. The system of claim 1 wherein the system bridge controller includes a CPU interface block for coupling the CPU to the MPEG video decoder and the means for displaying the video.

15. The system of claim 14 wherein the CPU interface block is coupled with the CPU selected from a group consisting of a MIPS processor, an SH3 processor and an SH4 processor.

16. The system of claim 14 wherein the CPU interface block is capable of performing burst accesses of the CPU in both read and write directions.

17. The system of claim 14 wherein the CPU interface block includes one or more buffers used to resolve a speed difference between the CPU and external SDRAM devices.

18. The system of claim 14 wherein the CPU interface block is capable of performing format conversion between big-endian data used in the CPU and little-endian data used in at least one of the MPEG video decoder and the means for displaying the video.

19. The system of claim 14 wherein the CPU interface block is capable of performing format conversion between little-endian data used in the CPU and big-endian data used in at least one of the MPEG video decoder and the means for displaying the video.

20. The system of claim 1 wherein the video includes at least one HDTV video.

21. The system of claim 1 wherein the video includes at least one SDTV video.

22. A method of coupling a CPU to other devices comprising the steps of:

coupling the CPU to a plurality of peripheral devices via a system bridge controller having a north bridge function on an integrated circuit chip,

wherein the integrated circuit chip is used to process MPEG video data to generate video for displaying and to display the video, and

wherein the CPU and the plurality of peripheral devices are situated externally to the integrated circuit chip.

23. The method of coupling a CPU to other devices of claim 22 wherein the step of coupling the CPU to a plurality of peripheral devices comprises the step of performing format conversion between big-endian data and little-endian data, between the CPU and one or more of the plurality of peripheral devices.

24. The method of coupling a CPU to other devices of claim 22 wherein the integrated circuit chip contains one or more internal components, and the method further comprises the step of coupling the

CPU to at least one of the one or more internal components via the system bridge controller.

25. The method of coupling a CPU to other devices of claim 24 wherein the step of coupling the CPU to at least one of the one or more internal components comprises the step of performing format conversion between big-endian data and little-endian data, between the CPU and at least one of the one or more internal components.

26. The method of coupling a CPU to other devices of claim 22 wherein the step of coupling the CPU to a plurality of peripheral devices comprises the step of coupling the CPU to one or more PCI devices.

27. The method of coupling a CPU to other devices of claim 26 further comprising the step of performing a DMA function between the one or more PCI devices and an external memory.

28. The method of coupling a CPU to other devices of claim 26 wherein the step of coupling the CPU to one or more PCI devices comprises the step of performing format conversion between big-endian data used in the CPU and little-endian data used in the one or more PCI devices.

29. The method of coupling a CPU to other devices of claim 26 wherein the step of coupling the CPU to one or more PCI devices comprises the step of performing format conversion between little-endian data used in the CPU and big-endian data used in the one or more PCI devices.

30. The method of coupling a CPU to other devices of claim 22 wherein the step of coupling the CPU to a plurality of peripheral

devices comprises the step of coupling the CPU to one or more I/O devices.

31. The method of coupling a CPU to other devices of claim 30 wherein the step of coupling the CPU to one or more I/O devices comprises the step of performing a DMA function between the CPU and the one or more I/O devices.

32. The method of coupling a CPU to other devices of claim 30 wherein the one or more I/O devices include one or more devices selected from a group consisting of ROM, RAM, flash memory and 68000-compatible peripheral devices.

33. The method of coupling a CPU to other devices of claim 30 wherein the step of coupling the CPU to one or more I/O devices comprises the step of performing format conversion between big-endian data used in the CPU and little-endian data used in the one or more I/O devices.

34. The method of coupling a CPU to other devices of claim 30 wherein the step of coupling the CPU to one or more I/O devices comprises the step of performing format conversion between little-endian data used in the CPU and big-endian data used in the one or more I/O devices.

35. The method of coupling a CPU to other devices of claim 24 wherein the step of coupling the CPU to at least one of the one or more internal components comprises the step of performing burst accesses of the CPU in both read and write directions.

36. The method of coupling a CPU to other devices of claim 24 wherein the step of coupling the CPU to at least one of the one or

more internal components comprises the step of resolving a speed difference between the CPU and external SDRAM devices.

37. The method of coupling a CPU to other devices of claim 24 wherein the step of coupling the CPU to at least one of the one or more internal components comprises the step of performing format conversion between big-endian data used in the CPU and little-endian data used in at least one of the MPEG video decoder and the means for displaying the video.

38. The method of coupling a CPU to other devices of claim 24 wherein the step of coupling the CPU to at least one of the one or more internal components comprises the step of performing format conversion between little-endian data used in the CPU and big-endian data used in at least one of the MPEG video decoder and the means for displaying the video.

39. The method of coupling a CPU to other devices of claim 22 wherein the video includes at least one HDTV video.

41. A system comprising:

an MPEG Transport processor for receiving a plurality of MPEG Transport streams, at least one of the MPEG Transport streams including MPEG video data;

an MPEG video decoder for processing the MPEG video data to generate video for displaying;

means for displaying the video; and

a system bridge controller having a north bridge function for coupling a CPU to at least one of the MPEG Transport processor, the MPEG video decoder and the means for displaying the video, and to a plurality of peripheral devices,